REMARKS

Claims 7, 12-14, 25-26, 28-29 and 31 have been canceled. Claims 1-6, 8-11, 15-24, 27, 30 and 32 remain pending in the application.

Claims 1-25, 27-30 and 32 were rejected under 35 U.S.C 102(b) as being anticipated by Chonan.

Turning first to claim 1, Applicant has amended claim 1 to include the limitation of the delay circuit. More specifically, the delay circuit is coupled to delay application of the enable signal to the regulator circuit, but not the circuit, so that the circuit is enabled/disabled for the operation prior to the response of the regulator circuit in providing the first/second current values, respectively.

The Examiner has indicated, in rejecting dependent claims 6-8 that Chonan teaches the claimed delay component and operation. In support, the Examiner points to an un-shown delay component in circuit 200 and the timing diagram of Figure 5. Applicant respectfully disagrees.

Chonan Figure 5 illustrates that the phi0 signal is turned active high by circuit 200 at the same time as RAS-not (the asserted "enable signal") goes low. There accordingly is no delay of the RAS-not signal with respect to its application (through the phi0 signal) to the power circuits 1 and 2 (i.e., the claimed "regulator circuit"). Additionally, Figure 5 shows that when the RAS-not signal later goes low, that the phi0 signal goes high at the same time. Thus, again, there is no delay of the RAS-not signal with respect to its application (through the phi0 signal) to the power (regulator) circuits 1 and 2. In summary, it is clear from Chonan Figure 5 that the system of Figure 4 is designed to have the circuit 200/100 and the power circuits 1 and 2 respond simultaneously to state changes in the RAS-not signal. This is contrary to the claimed operation.

It is noted that the phi1 and ph2 signals, and their effects on the power circuits 1, 2 and 3 of Chonan Figure 4, are not relevant to claim 1 since the claim clearly recites that the regulator circuit is operable responsive to the enable signal (i.e., RAS-not) to selectively provide a current to the circuit at a first current value when the enable signal is in the first state and at a second current value when the enable signal is in the second state. The only circuit operation in Chonan which could meet the recited regulator circuit operation, with respect to the state of the RAS-not signal, relates to the power circuits 1 and 2 along with the influence of the phi0 signal. The phi1 and phi2 signals, which have go low state changes unrelated to the RAS-not state changes are therefore not relevant to the claimed invention.

In view of the foregoing, and more specifically the failure of the Chonan circuit to disclose, teach or suggest a delay circuit and its claimed operation to delay application of the enable signal to the regulator circuit, but not the circuit, so that the circuit is enabled/disabled for the operation prior to the response of the regulator circuit in providing the first/second current values, Applicant respectfully submits that claim 1 is patentable over the cited prior art.

Claim 11 has been amended to recite that the regulator circuit comprises a first current source relating to the relatively lower non-zero current level and a second current source relating to the relatively higher non-zero current level, the first and second current sources comprising reference legs within a common current mirror circuit, the second current being selectively actuated when the enable input is in the first state. Applicant respectfully submits that Chonan fails to disclose, teach or suggest the claimed configuration for the regulator circuit.

With reference to Chonan Figure 4, there is presented a regulator circuit comprised of a plurality of power circuits 1-3. What is important to note is that power circuit 1 includes a first

current source for supplying the relatively lower non-zero current I1 when the enable signal (RAS-not) is in the second state (i.e., is high). Chonan then uses power circuit 2 having a second current source in order to generate an additional current I12 that is added to current I1 in order to supply the relatively higher non-zero current when the enable signal RAS-not is in the first state (i.e., is active low). The first and second current sources in Chonan Figure 4 are in separate power circuit 1 and 2 and thus do NOT, as is claimed, comprise "reference legs within a common current mirror circuit." There is no teaching or suggestion in Chonan for such a configuration with respect to the lower and higher non-zero currents relating to the states of the RAS-not enable signal. Clearly, with respect to RAS-not driven actuation, Chonan teaches away from the claimed configuration by having the relatively lower non-zero current be generated in a separate power circuit. Claim 11 is accordingly submitted as being patentable over the cited prior art.

Claim 21 is a method claim that is analogous to claim 1 and believed to be patentable over the cited Chonan reference for at least the same reasons as claim 1.

Claim 27 is a method claim that is analogous to claim 11 and believed to be patentable over the cited Chonan reference for at least the same reasons as claim 11.

Applicant respectfully submits that the application is in condition for favorable action and allowance.

Respectfully submitted,
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